

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Davis, Henry)
)
Appl. No. : To be assigned)
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Filed : Herewith)
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For : **DSP BUS MONITORING**)
 APPARATUS AND METHOD)
)
Examiner : Unknown)
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Group : Unknown)
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)
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)



27299
PATENT TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing forty-four (44) references, all of which were previously disclosed to or cited by the Patent and Trademark Office in the prosecution of U.S. patent application Serial No. 09/638,461, filed August 14, 2000, which will issue on September 9, 2003, as U.S. Patent No. 6,618,775; and patent application Serial No. 09/026,734 filed February 20, 1998, which is the parent of the continuation application, and is relied upon for an earlier filing date under 35 U.S. C. 120. Copies of these references are not submitted pursuant to 37 C.F.R. §1.98(d).

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Pursuant to 37 C.F.R. § 1.97(g) and (h), Applicant makes no representation that a search has been made or that the information cited is considered to be material to patentability. Additionally, inclusion on this list is not an admission that any of the cited documents are prior art in this application. Further, Applicant makes no representation regarding the completeness of this list or that better art does not exist.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: September 5, 2003

By: 

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. SEARCHP.005C2	APPLICATION NO. To be assigned
	APPLICANT Henry A. Davis	
	FILING DATE herewith	GROUP Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1	5,142,673	8/25/92	DeAngelis, et al.	395	575	
	2	5,210,862	5/11/93	DeAngelis, et al.	395	575	
	3	5,313,618	5/17/94	Pawloski	395	500.49	
	4	5,325,368	6/28/94	James, et al.	714	727	
	5	5,329,471	7/12/94	Swoboda, et al.	395	500.44	
	6	5,355,369	10/11/94	Greenberger Alan J., et al.	714	724	
	7	5,371,551	12/1994	Logan, et al.	348	571	
	8	5,375,228	12/20/94	Leary, et al.	710	33	
	9	5,463,760	10/31/95	Hamauchi	395	500.49	
	10	5,488,688	1/30/96	Gonzales, et al.	710	34	
	11	5,513,338	4/30/96	Alexander, et al.	395	500.49	
	12	5,530,804	6/25/96	Edgington, et al.	710	30	
	13	5,535,412	7/1996	Nadehara	711	110	
	14	5,539,901	7/23/96	Ramirez	395	500.49	
	15	5,544,311	8/6/96	Harenberg, et al.	714	40	
	16	5,546,566	8/13/96	Katsuta	395	500.49	
	17	5,560,036	09/24/96	Yoshida	395	500.44	
	18	5,561,761	10/1/96	Hicok, et al.	714	30	
	19	5,566,303	10/15/96	Tashiro, et al.	710	100	
	20	5,590,354	12/31/96	Klapproth, et al.	714	30	
	21	5,610,826	3/11/97	Whetsel	364	487	
	22	5,621,651	4/15/97	Swoboda	395	500.44	
	23	5,623,673	4/22/97	Gephardt, et al.	710	260	
	24	5,631,910	5/20/97	Nozuyama, et al.	714	724	
	25	5,640,542	6/17/97	Whitsel, et al.	395	500.49	
	26	5,671,172	9/1997	Britton	365	45	
	27	5,729,678	3/17/98	Hunt, et al.	395	183.19	
	28	5,812,830	9/1998	Naasch-Shahry et al.			
	29	5,908,392	6/1999	Wilson, et al.	600	509	
	30	5,960,457	9/28/99	Skrovan, et al.	711	146	

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	APPLICANT Henry A. Davis	
	FILING DATE herewith	GROUP Unknown

U.S. PATENT DOCUMENTS – cont.							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	31	5,999,163	12/1999	Ivers, et al.	345	134	
	32	6,026,503	2/2000	Gutgold et al.			

FOREIGN PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	
	33	Duane R. Aadsen, Harold N. Scholz, and Yervant Zorian; <u>Automated Bist for Regular Structures Embedded in Asic Devices</u> ; <i>AT&T Technical Journal</i> , May/June 1990; Pages 97-109
	34	D. Mukherjee, C. Njinda and M.A. Breuer; <u>Synthesis of Optimal 1-Hot Coded On-Chip Controllers for BIST Hardware</u> ; <i>IEEE International Conference on Computer-Aided Design</i> ; November 1991; Pages 236-239
	35	IEEE Computer Society; <u>IEEE Standard Test Access Port and Boundary-Scan Architecture</u> ; October 1993
	36	Debaditya Mukherjee, Massoud Pedram, and Melvin Breuer; <u>Merging Multiple FSM Controllers for DFT/BIST Hardware</u> ; <i>IEEE/ACM International Conference on Computer-Aided Design</i> ; November 1993; Pages 720-725
	37	Vishvani D. Agrawal, Chih-Jen Lin, Paul W. Rutkowski, Shianling Wu, and Yervant Zorian; <u>Built-In Self-Test for Digital Integrated Circuits</u> ; <i>AT&T Technical Journal</i> , March/April 1994; Pages 30-39
	38	Sybil Hellebrand, Hans-Joachim Wunderlich; <u>An Efficient Procedure for the Synthesis of Fast Self-Testable Controller Structures</u> ; <i>IEEE/ACM International Conference on Computer-Aided Design</i> ; November 1994; pages 110-116
	39	Albrecht P. Stroele and Hans-Joachim Wunderlich; <u>Test Register Insertion with Minimum Hardware Cost</u> ; <i>IEEE/ACM International Conference on Computer-Aided Design</i> ; November 1995; pages 95-101
	40	Takeshi Ikenaga and Takeshi Ogura; <u>A Distributed BIST Technique and Its Test Design Platform for VLSIs</u> ; <i>IECE Trans. Electron.</i> ; Vol. E78-C, No. 11; November 1995; Pages 1618-1623
	41	Miodrag Potkonjak, Sujit Dey, Kazutoshi Wakabayashi; <u>Design-For-Debugging of Application Specific Designs</u> ; <i>IEEE/ACM International Conference on Computer-Aided Design</i> ; November 1995; Pages 295-301
	42	Dan Strassberg; <u>BIST: Pie in the Sky No Longer</u> ; <i>EDN</i> ; September 1996; Pages 77-85
	43	Karim Arabi, Bozena Kaminska and Janusz Rzeszut; <u>BIST for D/A and A/D Converters</u> ; <i>IEEE Computer Society</i> ; Winter 1996; Pages 49-49
	44	<u>The Right Tools Do the Best Jobs</u> ; <i>EDN</i> ; June 1997; Pages S-10 - S-21

EXAMINER	DATE CONSIDERED
*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.	